

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would again like to thank the Examiner for allowing Claims 22-34, and for correctly indicating as allowable the subject matter of dependent Claims 8-20 and 40-42. Independent Claim 7 has been amended to more clearly define the present invention over the cited prior art references. The arguments supporting patentability of the claims are presented in detail below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 7 and 35 over the Argyroudis patent in view of the Santore et al. patent. The present invention, as recited in amended independent Claim 7, for example, is directed to a data transceiver station comprising a modem to be connected to an electrical power line.

The electrical power line receives digital data, a microprocessor is connected to the modem for receiving demodulated digital data therefrom according to a Packet Mode transmission or a Bit Mode transmission, and an interface circuit is connected between the microprocessor and the modem. The interface circuit switches between a Packet Mode and a Bit Mode during transfer of the demodulated digital data to the microprocessor. The switching is based upon whether the received digital data is a Packet Mode transmission or a Bit Mode transmission. The data transceiver station in accordance with the claimed invention advantageously joins together the advantages of a Packet Mode transmission with the advantages

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

of a Bit Mode transmission received over an electrical power line.

Independent method Claim 35 is similar to amended independent device Claim 7, and all ready recites that the digital data is exchanged over an electrical power line.

Referring now to FIG. 2 of the Argyroudis patent, the Examiner has characterized the data transceiver station as comprising a modem 226, 234 connected to a transmission line 228, 230, and a microprocessor 214 connected to the modem. The transmission line 228, 230 is an electrical power line. An interface circuit 224 is connected between the microprocessor 214 and the modem 226, 234.

As correctly noted by the Examiner, Argyroudis fails to disclose that the interface circuit 214 is capable of operating between a Packet Mode transmission and a Bit Mode transmission. However, the Examiner notes that the interface circuit 224 "may further comprise an embedded UART for transmitting at higher data rates over twisted pair transceiver 234." (Column 12, lines 39-42.) The Examiner has taken the position that Argyroudis is capable of communicating between two modes of data rates. The higher data rate is over the twisted pair transceiver 234 and the lower data rate is over the power line transceiver 226.

The Examiner cited the Santore et al. patent as disclosing a communications system having an interface card 30d operating between a Packet Mode transmission and a Bit Mode transmission. The Examiner has taken the position that it would have been obvious to modify the interface circuit 224 in Argyroudis based upon Santore et al. to extend the

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

operating capability of the data transceiver station disclosed therein since it could operate in two modes, i.e., a Packet Mode and a Bit Mode.

Even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. In the claimed invention, digital data is received over an electrical power line connected to the modem. The digital data received over the electrical power line is in one of two modes: a Packet Mode or a Bit Mode. Consequently, the interface circuit connected to the modem in the claimed invention switches between the Packet Mode and the Bit Mode during transfer of the demodulated data from the modem to the microprocessor based upon the digital data received over the electrical power line. In sharp contrast, the two modes of data rates in Argyroudis are received over two different paths. The higher data rate is received over a twisted pair line 232, whereas the lower data rate is received over the electrical power lines 228, 230.

It also appears that the Examiner is using impermissible hindsight reconstruction to modify Argyroudis in view of Santore et al. in an attempt to produce the claimed invention. The Applicants respectfully assert that obvious cannot be established by combining the teachings of Argyroudis in view of Santore et al. in an attempt to produce the claimed invention without some proper prior art teaching, suggestion or incentive supporting such a combination.

The Applicants respectfully submit that Argyroudis teaches away from such a combination because the digital data received by the modem 234, 226 is received at one rate over an electrical power line 228, 239 and received at a different

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

rate over a twisted line pair 232. Moreover, even though the interface circuit 224 in Argyroudis supports a higher data rate, the Examiner arbitrarily associates this higher data rate with a Packet Mode transmission. However, such an association appears to be backwards. The Examiner associated the higher data rate (i.e., Packet Mode) over the twisted line pair 232, whereas this type of transmission would normally be over the electrical power line 228, 239. Consequently, the higher data rate in Argyroudis must be for a different type of transmission. In other words, Argyroudis fails to teach or suggest that the interface circuit 224 supports a Bit Mode transmission and Burst Mode transmission during transfer of data to the microprocessor 214.

In Santore et al., the disclosed interface card 30d supporting Packet Mode transmission and Bit Mode transmission interface is not connected between a modem and a processor, as in the claimed invention. Instead, the interface card 30d is based upon multiple RISC processors which provide packet switching and LAN internetworking, and is connected between a backplane bus 20 and a LAN network, as illustrated in FIG. 1. The prior art references, individually, or in combination, do not teach or suggest such a combination.

Accordingly, it is submitted that amended independent Claim 7 is patentable over Argyroudis in view of Santore et al. Independent Claim 35 is similar to amended independent Claim 7. Therefore, it is also submitted that this claim is also patentable over Argyroudis in view of Santore et al. In view of the patentability of the independent Claims 7 and 35, it is submitted that their dependent claims, which recite yet further distinguishing

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

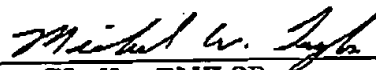
features of the invention, are also patentable. These
dependent claims require no further discussion herein.

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. 09/699,041
Filing Date: October 27, 2000

CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,


MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 24 day of February, 2004.

